AMENDMENT TO THE SPECIFICATION

At page 3, please replace paragraph [0007] with the following:

[0007] Fig. 1 shows a substrate 11 having a doped well over which the memory cells are formed. The substrate can be formed of any semiconductor material with silicon being exemplary. The substrate 11 has fabricated thereon a plurality of gate stacks, two of which (13b and 13c) are part of MOSFET access transistors 15a and 15b for lower memory cells of the stacked pairs of cells. Transistors 15a and 15b have associated source/drain doped regions 17a, 17b, and 17c. The gate stacks each contain an oxide layer, e.g. a silicon oxide layer 21, in contact with substrate 11, a conductor layer 23 formed of, for example, polysilicon, a conductive silicon layer 25 and a cap insulating layer 27 formed of, for example, silicon nitride. Insulating sidewall ~~spaces~~ spacers 29 of, for example, silicon nitride are also provided. The material composition of the various layers and sidewalls of the gate stacks is not critical as other well known materials used to form the components of a transistor gate stack may also be used.

At page 6, please replace paragraph [0013] with the following:

[0013] The specific binary values stored within the memory cells 118, 120 of the present invention is determined by respective sense amplifiers 159, 180. As shown in Fig. 7, the PCRAM system of the present invention locates those sense amplifiers 159 and 180 in the periphery of the memory array of the present invention. Using memory cell 118 as an example, a sense amplifier 159 has one input tied to the common anode 110, and the other input tied to the access transistor 118_{AT} device through a column line A through a transistor 150. The access transistor 118_{AT} is connected to a wordline and allows charge to move from the memory cell 118 to the sense amplifier 159 when both row and columns associated with cells 118, 120 are selected, and the lower cell 118 is selected. As an alternative to being tied to common anode 110, the input 158 of sense amplifier 159 can instead be tied to a reference signal which may be another inactive column line.

AMENDMENT TO THE CLAIMS

1-16 (Cancelled)

17. (Currently Amended) A method of fabricating a memory device comprising:

forming a first memory cell ~~to include~~ comprising a resistance-changeable chalcogenide glass material ~~having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material~~ between and electrically coupled to a first electrode and a second electrode; and

forming a second memory ~~cells as a commode to include~~ cell comprising a resistance-changeable chalcogenide glass material ~~having a changeable resistance and cathode and anode electrodes spaced apart and in contact with said chalcogenide glass material~~ between and electrically coupled to said second electrode and a third electrode;

~~forming said anode electrodes of said memory cells as a common anode,~~ wherein said ~~common anode comprises a middle conductive layer and a layer of silver on opposite sides of said middle conductive layer~~ second electrode comprises a first silver layer, a tungsten layer over said first silver layer, and a second silver layer over said tungsten layer.

18. (Currently Amended) A method as in claim 17 further comprising~~: forming~~ vertically stacking said first memory cell ~~such that it is stacked on~~ and said second memory cell.

19.(Currently Amended) A method as in claim 17 ~~further comprising: forming each of said first and second memory cells of a layered structure which includes a cathode layer, a chalcogenide glass material layer having a changeable resistance and a anode layer~~ , wherein said first and third electrodes each comprise a layer of tungsten and a layer of tungsten nitride.

20. (Currently Amended) A method as in claim 17, wherein each of said ~~cathodes~~ first and third electrodes comprises ~~a~~ at least one layer of tungsten, platinum, titanium, cobalt, aluminum, or nickel.

21. (Cancelled)

22. (Currently Amended) A method as in claim 17, wherein said ~~middle conductive layer comprises tungsten~~ first electrode, said second electrode, and said third electrode are each electrically coupled to a voltage source or to a read circuit.

23. (Currently Amended) A method as in claim 18 further comprising: forming said stacked first and second memory cells over a conductive plug such that said ~~cathode~~ first electrode of said ~~second~~ first memory cell is ~~in~~ electrically coupled ~~with~~ to said conductive plug.

24. (Currently Amended) A method as in claim ~~23~~ 18 further comprising:

forming a first row line conductor ~~electrically coupled to a second active region of a first access transistor~~ to control current flow between a first column line and said first electrode;

forming a second row line conductor to control current flow between a second column line and said third electrode; and

forming a sense amplifier circuit electrically coupled to said second electrode.

25. (Currently Amended) A method as in claim ~~23~~ 17, ~~further comprising forming a word line conductor which is electrically coupled to a gate of a first access transistor~~ wherein said chalcogenide glass material of said first and second memory cells comprises germanium selenide.

26. (Currently Amended) A method as in claim ~~23~~ 25, ~~further comprising forming a second access transistor and electrically coupling said second access transistor to said second memory cell~~ wherein said germanium selenide has the formula $(Ge_xSe_{1-x}) + Ag$.

27. (Currently Amended) A method as in claim ~~26~~ 17, wherein said first and second memory cells are ~~formed to be~~ coupled to different column lines by ~~said~~ respective first and second access transistors.

28. (Currently Amended) A method as in claim 17, wherein said first and second memory cells are ~~formed to be connected to the same~~ electrically coupled to a single column line by ~~said~~ respective first and second access transistors.

29. (Currently Amended) A method as in claim ~~26~~ 28 further comprising: forming a circuit for operating said first and second access transistors ~~separately~~ to individually access each of said first and second memory cells.

30. (Currently Amended) A method as in claim ~~17~~ 28 further comprising: forming a circuit for operating said first and second access transistors ~~together~~ to access both said first and second memory cells simultaneously.

31-57. (Cancelled)

58. (Currently Added) A method of forming a memory device comprising:

forming a first electrode, said first electrode comprising a material selected from the group consisting of tungsten, tungsten nitride, platinum, titanium, cobalt, aluminum, and nickel;

forming a first germanium selenide layer over and electrically coupled said first electrode;

incorporating a first silver-containing material into said first germanium selenide layer;

forming a first silver layer over and electrically coupled to said first germanium seleinde layer;

forming a tungsten layer over and electrically coupled to said first silver layer;

forming a second silver layer over and electrically coupled to said tungsten layer;

forming a second germanium selenide layer over and electrically coupled to said second silver layer;

incorporating a second silver-containing material into said second germanium selenide layer; and

forming a second electrode over and electrically coupled to said second germanium selenide layer, said second electrode comprising a material selected from the group consisting of tungsten, tungsten nitride, platinum, titanium, cobalt, aluminum, and nickel.

59. (Currently Added) A method of fabricating a memory device comprising:

forming a first memory cell comprising a resistance-changeable chalcogenide glass material between and electrically coupled to a first electrode and a second electrode;

forming a second memory cell comprising a resistance-changeable chalcogenide glass material between and electrically coupled to said second electrode and a third electrode;

providing a first access circuit for said first memory cell, said first access circuit comprising a first column line, a first row line, and a first access transistor having a gate

coupled to said first row line and configured to electrically couple said first electrode to said first column line; and

providing a second address circuit for said second memory cell, said second address circuit comprising a second column line, a second row line, and a second access transistor having a gate coupled to said second row line and configured to electrically couple said third electrode to said second column line.

60. (Currently Added) The method of claim 59, further comprising providing a first sense amplifier circuit electrically coupled to said first column line and a second sense amplifier circuit electrically coupled to said second column line.

61. (Currently Added) The method of claim 60, further comprising:

providing a third transistor between said first column line and said first sense amplifier circuit; and

providing a fourth transistor between said second column line and said second sense amplifier circuit.

62. (Currently Added) The method of claim 59, further comprising providing a sense amplifier circuit electrically coupled to said second electrode.

REMARKS

Applicant acknowledges with appreciation the allowance of claims 17-20 and 22-27 and the indication of allowability of claims 28-30. The specification is amended to correct minor clerical errors; a misspelled word in paragraph [0007] and a punctuation error in paragraph [0013]. Claims 17-20 and 22-30 are amended to more clearly define the subject matter of the invention, not for any reasons relating to patentability. New claims 58-62 are added. Claims 1-17, 21, and 31-57 are cancelled without prejudice to their underlying subject matter. Concurrently herewith is submitted a substitute formal drawing for FIG. 1 in accordance with the approved changed drawings.

Claims 28-30 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. This rejection is respectfully traversed. The amendment to these claims should place the claims in condition for allowance. The 35 U.S.C. § 112, second paragraph, rejection of claims 28-30 is respectfully requested to be withdrawn.

Claims 47-54 and 57 stand rejected under 102(e) as being anticipated by U.S. application, publication number 2002/0168820 (Kozicki et al.). These claims are cancelled and thus this rejection is moot. However, Applicant would like to direct the Examiner's attention to Kozicki et al. paragraphs [0099] through [0102] referring to figures 25-29. The common electrode structures disclosed by Kozicki et al. do not anticipate or render obvious the subject matter of the currently pending claims 17-20, 22-30, and 58-62.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

Dated: June 30, 2003

Respectfully submitted,

By_____

Thomas J. D'Amico
Registration No.: 28,371
Ryan H. Flax
Registration No.: 48,141
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L Street NW
Washington, DC 20037-1526
(202) 785-9700
Attorneys for Applicant